Customer No.: 31561
Docket No.: 10465-US-PA
Application No.: 10/707,354

REMRAK

Claims 1-5, 7-8 and 19-21 are pending of which the claim 19 has been amended without prejudice or disclaimer in order to more explicitly describe the claimed invention. It is believed that no new matter is added by way of amendments made to claims. For at least the foregoing reason, Applicants respectfully submit that claims 1-5, 7-8 and 19-21 patently define over prior art of record and reconsideration of this application is respectfully requested.

Discussion for rejection to claims under 35U.S.C. 112 1st and 2nd paragraphs

3. *Claims 1-5, 7 and 8 are rejected under 35 U.S.C. 112 2nd paragraph, as being indefinite for failing to particularly point out the subject matter the applicant regards as the invention.*

5. *The amendment filed on 1/16/06 is objected to under 35 U.S.C. 132(a) because it introduces new matter, i.e. the recitation of the push/pull signal being level shifted.*

6. *Claims 1-5, 7 and 8 are rejected under 35 U.S.C. 112 1st paragraph, as failing to comply with the written requirement due to the presence of new matter.*

In response thereto, applicant respectfully traverses new matter,

i.e. the recitation of the push/pull signal being level shifted, based on the following two references that is to be filed as IDS of the present invention, and arguments. Furthermore, the claim 5 should not be rejected on the grounds of presence of new matter because it has no such new matter. The first reference is a textbook, titled "INTRODUCTION TO CMOS OP-AMPS AND COMPARATORS," written by ROUBIK GREGORIAN. In the next page, the first two sentences in chapter 3.4(i.e. page 74) disclose "MOS source followers are similar to bipolar emitter followers. They can be used as buffer or as dc level shifters," wherein the MOS source followers take NMOS as an example. Moreover, the sixth NMOS transistor 306 and the current source 310 of the present invention are identical to Q1 and Q2 transistors, respectively, which constitute a MOS source follower as shown in Fig.3.33, in page 75. The signal received at the gate of the sixth NMOS transistor 306 is functionally identical to Vin shown in Fig.3.33.

Customer No.: 31561
Docket No.: 10465-US-PA
Application No.: 10/707,354

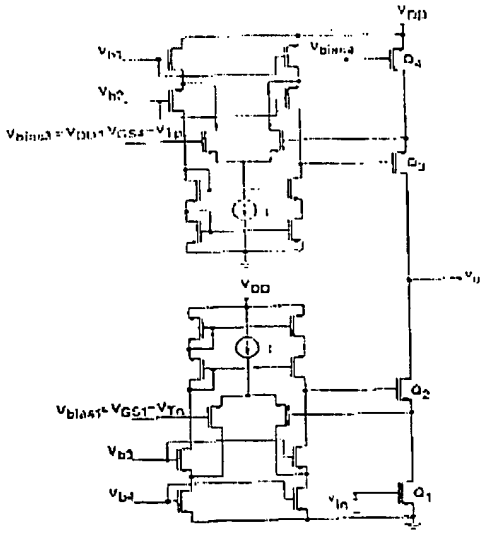

Figure 3.32. Complete circuit diagram of a gain-enhanced cascode amplifier employing folded-cascode op-amps as feedback amplifiers.

3.4. MOS SOURCE FOLLOWERS [5–8]

MOS source followers are similar to bipolar emitter followers. They can be used as buffers or as dc level shifters. The basic source follower, with an NMOS input device and an NMOS current source as an active load, is shown in Fig. 3.33 and its small-signal low-frequency equivalent circuit in Fig. 3.34. The node current equation for the output node is

$$(g_{ds1} + g_{ds2})v_{out} + |g_{ms4}|v_{out} - g_{m2}v_{gs1} = 0. \tag{3.65}$$

Substituting $v_{gs1} = v_{in} - v_{out}$ and solving yields

$$A_v = \frac{v_{out}}{v_{in}} = \frac{g_{m1}/(g_{ds1} + g_{ds2}|g_{ms4}|)}{g_{m1}/(g_{ds1} + g_{ds2} + |g_{ms4}|) + 1}. \tag{3.66}$$

Hence $A_v \approx 1$ if $g_{m1} \gg g_{ds1} + g_{ds2} + |g_{ms4}|$.

Customer No.: 31561
Docket No.: 10465-US-PA
Application No.: 10/707,354

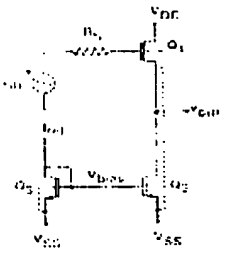

Figure 3.33 Basic structure of MOS source follower.

The output impedance of the source follower can be calculated by applying a test source v_x at its output (Fig. 3.35). The current law gives

$$i_x = (g_{m2} + g_{mb2})v_x + |g_{mb1}|v_x - g_{m1}v_{gs1} \tag{3.67}$$

Here $v_{gs1} = -v_x$, and hence Eq. (3.67) gives

$$R_{out} = \frac{v_x}{i_x} = \frac{1}{g_{m2} + g_{mb2} + |g_{mb1}|} \approx \frac{1}{g_{m2}} \tag{3.68}$$

since usually $g_{m1} \gg g_{m2}$, g_{mb2}, and $|g_{mb1}|$. Thus R_{out} has a relatively low value, on the order of 1 kΩ.

The dc bias current of the stage is determined by the current source Q_2, which drives Q_1 at its low-impedance source terminal. Thus the dc drop V_{GS1} between the input and output terminals is determined by V_{bias} and the dimensions of Q_1 and Q_2; those parameters can be used to control the level shift provided by the stage.

The gate of the load device Q_2 may be connected to its drain to eliminate the

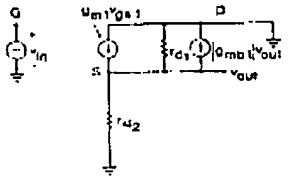

Figure 3.34 Small-signal low-frequency equivalent circuit of the source follower.

The second reference is US Patent No.6,903,539B1, which also shows a current source 500 makes use of a pair of source-follower (S-F) **level shifters 505 and 510.** Moreover, from the "ABSTRACT," there discloses " A preferred embodiment comprises a casecode current source arranged in a current mirror configuration (such as current source 600) with a pair of level shifters arranged in a source-follower..." Thus, it is well known that a source-follower is capable of level shifting functionality.

Customer No.: 31561
Docket No.: 10465-US-PA
Application No.: 10/707,354

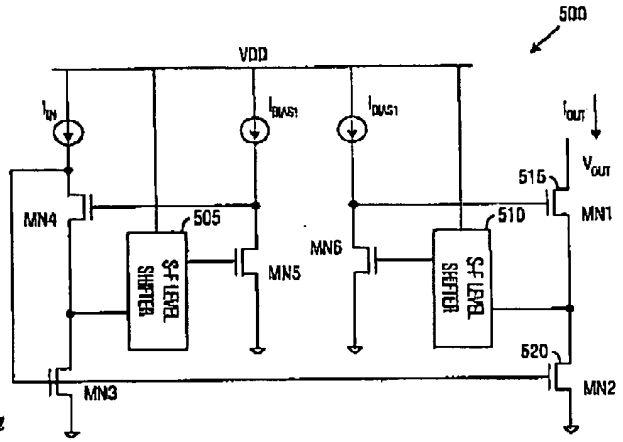

Fig. 5a

In accordance with the preceding description, please refer to the next page that shows two embodiments of the present invention. Accordingly, in Figs.2 and 3 of the present invention, a first push signal Vg1 at node 23 is level-shifted by a fifth PMOS transistor 304 (or V1 208 shown in Fig.2) to be a signal at node 26 (or signal presented at the negative terminal of V1 208 shown in Fig.2), and the first pull signal Vg2 at node 24 is also level-shifted by a sixth NMOS transistor 306 (or V2 210 shown in Fig.2) to be a signal at node 27 (or signal presented at the negative terminal of V2 210 shown in Fig.2). Furthermore, the second push signal Vg3 has the same electrical potential as node 26 (or as the negative terminal of V1 208 shown in Fig.2), and so does the second pull signal Vg4. In other words, as the first push signal Vg1 and the first pull signal Vg2 are output

of a differential amplifier 202, the second push signal Vg3 is level shifted from the first push signal Vg1 (or level shifted from the output from the differential amplifier 202), as well as, the second pull signal Vg4 is level shifted from the first pull signal Vg2 (or level shifted from the output from the differential amplifier 202). Thus, a recitation of the push/pull signals being level shifted, which is added to the claim 1, can not be regarded as "new matter."

Customer No.: 31561
Docket No.: 10465-US-PA
Application No.: 10/707,354

Discussion for rejection to claims under 35U.S.C. 103 (a)

7.Claims 1-5,7-8 are rejected under 35 U.S.C. 103 (a) as being unpatentable over any one of Miyabi, Kogushi, Hunt, Garcia and Sanwo in view of any one of Taguchi, Taito, Morishita and Cruz.

As to the new limitation that push-pull signals are level shifted, this not supported by the originally specification and therefore cannot be relied upon to distinguish over the prior art

As the aforementioned new limitation is explained as not new matter in the preceding section, applicant respectfully again traverses the preceding rejection based on the same arguments as response to FIRST OFFICE ACTION. The arguments emphasize neither the first group prior art references, nor the second prior art references teach, suggest the desirability of making the combination. Particularly, the citation Hunt should not be used as prior art reference because in Fig.4, the assistant output stage(72, 74) is not controlled by the input signal, but controlled by buf 1~buf n which is independent from the input signal(46). The input signal of the assistant output stage depends on the input signal of the main output stage in claim 1. Besides, the input signal of Hunt is a digital signal, and the output is also a digital signal. But the input signals of claim of the main output stage and the assistant output stage are analog signals, and the input signal of the main output stage is outputted from a differential amplifier, which is not disclosed in Hunt. The main output stage of claim1 has a

quiescent DC biased current which is presented in the main output stage (50,54) of Hunt.

The alleged main output stage (P3,N2,P2 andN3) of Garcia is not function as main output stage. It is used to control the alleged assistant output stage(P1,N1) which is function as an output stage. It only has one output stage in Garcia, and it is digital input and digital output. However, there are two output stages in claim 1, the main output stage and the assistant output stage, which is different from the Garcia.

The alleged main output stage (4,5,6 and 7) of Kogushi is not function as main output stage, it is used to charge/discharge the capacitor (14) to control the alleged assistant output stage (10,11) which is function as an output stage. The input signals (PEN, NEN) and the output signal (OUT) are digital signals.

In Miyabe, it states in column 1, line 23-26 "This configuration is shown in FIG.6, where a CMOS inverter consisting of a p-channel MOS transistor 61 and an n-channel MOS transistor 62 has an output terminal OUT." The transistors 61 and 62 of Miyabe is not function as a main output stage, but an inverter. The input signal (IN) is a digital signal which is different from the input signal of claim 1, an analog signal output from the differential amplifier.

Thus, Hunt should not be combined with any of Taguchi, Taito, Morishita and Cruz because they teach a differential amplifier is coupled to input of the main output stage and thus, the replacement of

the differential amplifier with the assistant output stage in Hunt makes its combination with one of Taguchi, Taito, Morishita and Cruz unexpected success. Hence, neither the first group prior art references, especial for Hunt, nor the second prior art references teach, suggest the desirability of making the combination. Thus, claims 1-5, 7-8 are not rendered obvious by all prior art references and accordingly patentable.

To establish a prima facie case of obviousness, the prior art references should disclose all limitations of claims. Accordingly, even if any one of Miyabi, Kogushi, Garcia and Sanwo could be combined with any one of Taguchi, Taito, Morishita and Cruz, this proposal combination still fails to discloses" the main current further comprises a quiescent DC biased current," as claimed in the claim 1, and "the first push current and the first pull current further comprises a quiescent DC biased current," as claimed in the claim 5. Thus, the claims 1and 5 are not rendered obvious by the combination of any one of Miyabi, Kogushi, Garcia and Sanwo with any one of Taguchi, Taito, Morishita and Cruz, and thus patentable.

As to dependent claims 2-4 and 7-8, they should be patentable as a matter of law for the reason they contain all limitations of their corresponding patentable base claims 1 and 5.

8. Claims 19-21 are objected to as being dependent upon a rejected base claim, but would be allowable if written in independent form including all limitations of the base claim and

any intervening claims.

In response thereto, applicant appreciated the Examiner's conditional allowance of claims 19-21. Accordingly, the claim 19 is so amended to be rewritten in an independent form including all limitations of its base claim 1.

9. *Applicant's arguments filed on 1/16/06 have been considered but they are not persuasive.*

The further arguments set forth on page 13 through 16 of the 1/16/06 response are similarly not persuasive because they are not reflected in the claims.

In response thereto, applicant would like to specifically point out distinct features as claimed in the claims over the prior art references based on the following arguments. As discussed above, even if any one of Miyabi, Kogushi, Garcia and Sanwo could be combined with any one of Taguchi, Taito, Morishita and Cruz, this proposal combination still fails to discloses" the main current further comprises a quiescent DC biased current," as claimed in the claim 1, and "the first push current and the first pull current further comprise a quiescent DC biased current," as claimed in the claim 5.

Customer No.: 31561
Docket No.: 10465-US-PA
Application No.: 10/707,354

CONCLUSION

For at least the foregoing reasons, it is believed that all the pending claims 1-5, 7-8 and 19-21 of the invention patently define over the prior art and are in proper condition for allowance. Reconsideration of claims 1-5, 7-8 and 19-21 of the present application is respectfully requested. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

Respectfully submitted,

Date : August 17, 2006

Belinda Lee

Registration No.: 46,863

Jianq Chyun Intellectual Property Office
7th Floor-1, No. 100
Roosevelt Road, Section 2
Taipei, 100
Taiwan
Tel: 011-886-2-2369-2800
Fax: 011-886-2-2369-7233
Email: belinda@jcipgroup.com.tw
Usa@jcipgroup.com.tw